EN779

Digital Camera Processor

Security Camera HD-ISP with Built-in HD-SDI TX and EX-SDI

Version 1.1
Sep 26, 2016

Revision History

Version	Date	Description	Modified by
1.0	2016.08.23.	Initial release.	HJ Jung
1.1	2016.09.26	Updated DC Electrical Characteristics & Power Consumption	HJ Jung

Document Description

This is the document to describe a feature and register which is applied to EN779.

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Contents

1. General Descriptions & Features

1.1 General Descriptions

This is digital camera processor for security camera system. The main features include Wide Dynamic Range (WDR), Adaptive Contrast Enhancer (ACE), 3D Noise Reduction (3DNR), auto (AE, AF, AWB) control, digital zoom and built-in HD-SDI TX and EX-SDI.

1.2 Features

Image Signal Processing

- Advanced RGB Interpolator for High Resolution
- Wide Dynamic Range compensation (WDR)
  - 2 page ISP internal WDR(Max. 90dB)
  - Line by Line WDR(Max. 120dB)
- Adaptive Digital Noise Reducer (2D/3D)
- Adaptive Contrast Enhancer (ACE)
- Lens Shading Compensation
- Digital Zoom
- Defect Detection & Correction
- Optical detector (AE, AF, AWB)
- Edge enhancement
- Gamma Correction
- Hue Controller (8-Way)
- High Light Masking
- Flip / Mirror / Still
- Box OSD (32ea, solid effects, auto zoom)
- Polygon Privacy Masking (8ea, auto zoom)
- Font OSD (Scalable 24x16 font, Styling, Half)
- Motion Object Detector
- Image Output Mode
  - 10/20bit width Digital Interface
    BT.1120, SMPTE274M (720p, 1080p)
    Support built-in HD-SDI TX
    (Integrated Cable Driver, 270M/1.485G/2.97G)
  - CVBS: NTSC, PAL (720H, 960H)
- Logic PWM Output
- Simple Down Scalier
  (1080p -> 720p, 1440p -> 720p,
  1440p -> 1080p,)
- External Flash Memory Controller
- De-fog
- Digital Image Stabilization (DIS)
- Embedded EX-SDI 2.0 Encoder (Long Reach)
- Virtual 4 wire for upstream data
- 1 Channel DAC (CVBS)
- 4 Channel ADC

Sensor Interface

- 1.3M ~ 4M CMOS sensor
- Sub-LVDS (8CH) / HiSPi (TBD) / MIPI Interface
- Master / Slave mode
- Frame Rate
  - 2.0M: Max. 60p
  - 4.0M: Max. 30p

Multimedia Features

- On-chip Encoder for CVBS (1ch DAC)
- On-chip ADC (4ch mux type)
- On-chip MCU (EXRISC 1.0)
  - 32bit processor (Max 74.25 MHz)
  - Embedded Program SRAM (128Kbyte)
  - 16Kbyte (I) + 8Kbyte (D) cache
  - Timer, UART, SPI, PWM, Watchdog timer, GPIO (32ea), IIC

Power Management

- 1.8~3.3V I/O
- 1.2V Core Power

Operating Frequency

- Max. 74.25MHz - MCU
- Max. 148.5MHz - ISP
- Max. 180MHz – DDR SDRAM

Operating Temperature

- 0˚C ~ +70˚C

Package

- 144ball FBGA 10mm x 10

2. Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12
A	PCLK	XI0	GPIO14	GPIO23	VDDQ_DDR	GPIO4	GPIO5	JTMS	JTDO	RX0	TX0	EXTS
B	MCKO	RSTX	XI1	GPIO22	VDDC	VDDC	VDDC	VDDC	JTDI	JTRST	REXTD	GND
C	GPIO6	VDDQ_SS	VSI	HSI	GPIO7	GPIO8	GPIO13	GPIO31	CVBS	COMP	AVDD_SDI	SDIM
D	GND	GND	GND	GND	AVDD_LV33	AVDD_LVPLL	JTCK	VDDQ_BT	AVDD_SDI33	RSET	LF	SDIP
E	LDIM0	LDIP0	LDIP1	LDIM1	GND	GND	GND	VDDQ_BT	VDDQ_BT	CO7	CO9	CO8
F	LDIM2	LDIP2	LDIP3	LDIM3	GND	GND	GND	VDDQ	CO3	CO4	CO6	CO5
G	LDIMCK	LDIPCK	LDIM4	LDIP4	GND	GND	VDDC	VDDQ	DCKO	CO0	CO2	CO1
H	LDIP5	LDIM5	LDIP6	LDIM6	GND	VDDC	VDDQ_DDR	VDDQ	YO6	YO7	YO9	YO8
J	LDIP7	LDIM7	GPIO24	GND	JMODE	TP0	TP1	HSO	YO2	YO4	YO3	YO5
K	GPIO10	GPIO9	GPIO19	GPIO18	GPIO30	GPIO29	GPIO0	TP2	VSO	DENO	YO1	YO0
L	GPIO11	GPIO15	GPIO21	GPIO25	GPIO28	GPIO1	GPIO2	SFDQ0	SFDQ2	SFCKO	ADCI2	ADCI0
M	GPIO12	GPIO16	GPIO20	GPIO27	GPIO26	GPIO17	GPIO3	SFDQ1	SFDQ3	SFCSN	ADCI3	ADCI1

EN779 Pin Diagram (Top View)

3. I/O Information

3.1 Pin Description

No.	Name	I/O	Function	
B2	RSTX	I	System Reset	
A2	XI0	I	System Clock 0	
B3	XI1	I	System Clock 1	
J6	TP0	I	Test pin	
J7	TP1	I	Test pin	
K8	TP2	I	Test pin	
C3	VSI	IO	Vertical Sync in / output for Sensor	
C4	HSI	IO	Horizontal Sync in / output for Sensor	
A1	PCLK	I	Pixel clock from Sensor in Parallel mode	
B1	MCKO	O	Sensor Operating clock	
E2	LDIP0	I	Sub-LVDS positive lane 0	CSI-2 positive lane 0
E1	LDIM0	I	Sub-LVDS negative lane 0	CSI-2 negative lane 0
E3	LDIP1	I	Sub-LVDS positive lane 1	CSI-2 positive lane 1
E4	LDIM1	I	Sub-LVDS negative lane 1	CSI-2 negative lane 1
F2	LDIP2	I	Sub-LVDS positive lane 2	CSI-2 positive lane 2
F1	LDIM2	I	Sub-LVDS negative lane 2	CSI-2 negative lane 2
F3	LDIP3	I	Sub-LVDS positive lane 3	CSI-2 positive lane 3
F4	LDIM3	I	Sub-LVDS negative lane 3	CSI-2 negative lane 3
G4	LDIP4	I	Sub-LVDS positive lane 4	
G3	LDIM4	I	Sub-LVDS negative lane 4	
H1	LDIP5	I	Sub-LVDS positive lane 5	
H2	LDIM5	I	Sub-LVDS negative lane 5	
H3	LDIP6	I	Sub-LVDS positive lane 6	
H4	LDIM6	I	Sub-LVDS negative lane 6	
J1	LDIP7	I	Sub-LVDS positive lane 7	
J2	LDIM7	I	Sub-LVDS negative lane 7	
G2	LDIPCK	I	Sub-LVDS positive clock	CSI-2 positive clock
G1	LDIMCK	I	Sub-LVDS negative clock	CSI-2 negative clock
J8	HSO	IO	Horizontal sync in / output for back-end processor	
K9	VSO	IO	Vertical sync in / output for back-end processor	
K10	DENO	O	Data enable sync for Digital output	
G9	DCKO	O	Output clock for Digital output	
K12	YO0	O	Parallel Digital Y output 0	10Bit Digital YC output 0 (Grout0)
K11	YO1	O	Parallel Digital Y output 1	10Bit Digital YC output 1 (Grout0)
J9	YO2	O	Parallel Digital Y output 2	10Bit Digital YC output 2 (Grout0)

J11	YO3	O	Parallel Digital Y output 3	10Bit Digital YC output 3 (Grout0)
J10	YO4	O	Parallel Digital Y output 4	10Bit Digital YC output 4 (Grout0)
J12	YO5	O	Parallel Digital Y output 5	10Bit Digital YC output 5 (Grout0)
H9	YO6	O	Parallel Digital Y output 6	10Bit Digital YC output 6 (Grout0)
H10	YO7	O	Parallel Digital Y output 7	10Bit Digital YC output 7 (Grout0)
H12	YO8	O	Parallel Digital Y output 8	10Bit Digital YC output 8 (Grout0)
H11	YO9	O	Parallel Digital Y output 9	10Bit Digital YC output 9 (Grout0)
G10	CO0	O	Parallel Digital C output 0	10Bit Digital YC output 0 (Grout1)
G12	CO1	O	Parallel Digital C output 1	10Bit Digital YC output 1 (Grout1)
G11	CO2	O	Parallel Digital C output 2	10Bit Digital YC output 2 (Grout1)
F9	CO3	O	Parallel Digital C output 3	10Bit Digital YC output 3 (Grout1)
F10	CO4	O	Parallel Digital C output 4	10Bit Digital YC output 4 (Grout1)
F12	CO5	O	Parallel Digital C output 5	10Bit Digital YC output 5 (Grout1)
F11	CO6	O	Parallel Digital C output 6	10Bit Digital YC output 6 (Grout1)
E10	CO7	O	Parallel Digital C output 7	10Bit Digital YC output 7 (Grout1)
E12	CO8	O	Parallel Digital C output 8	10Bit Digital YC output 8 (Grout1)
E11	CO9	O	Parallel Digital C output 9	10Bit Digital YC output 9 (Grout1)
D12	SDIP	O	HD-SDI positive output signal	
C12	SDIM	O	HD-SDI negative output signal	
D10	RSET	I	1% 750Ω resistor needs to be located between RSET and AVDD_LV33 on a board.	
D11	LF	I	100nF capacitor needs to be located between LF and GND without VIA.	
C9	CVBS	O	DAC output for CVBS	
C10	COMP	O	10uF capacitor needs to be located between COMP and GND on a board	
B11	REXTD	I	12.3kΩ(TBD) resistor needs to be located between REXTD and GND on a board	
A12	EXTS	I	External control signal input via CVBS	
A8	JTMS	I	JTAG data enable	
A9	JTDO	O	JTAG data output	
B9	JTDI	I	JTAG data input	
B10	JTRST	I	JTAG Reset, Active low	
D7	JTCK	I	JTAG clock	
J5	JMODE	I	10kΩ resistor needs to be located JMODE and VDDQ	
A10	RX0	I	UART Receive input	
A11	TX0	O	UART transmit output	
L12	ADCI0	I	Internal ADC input 0	
M12	ADCI1	I	Internal ADC input 1	
L11	ADCI2	I	Internal ADC input 2	
M11	ADCI3	I	Internal ADC input 3	
L10	SFCKO	O	External Serial flash clock	

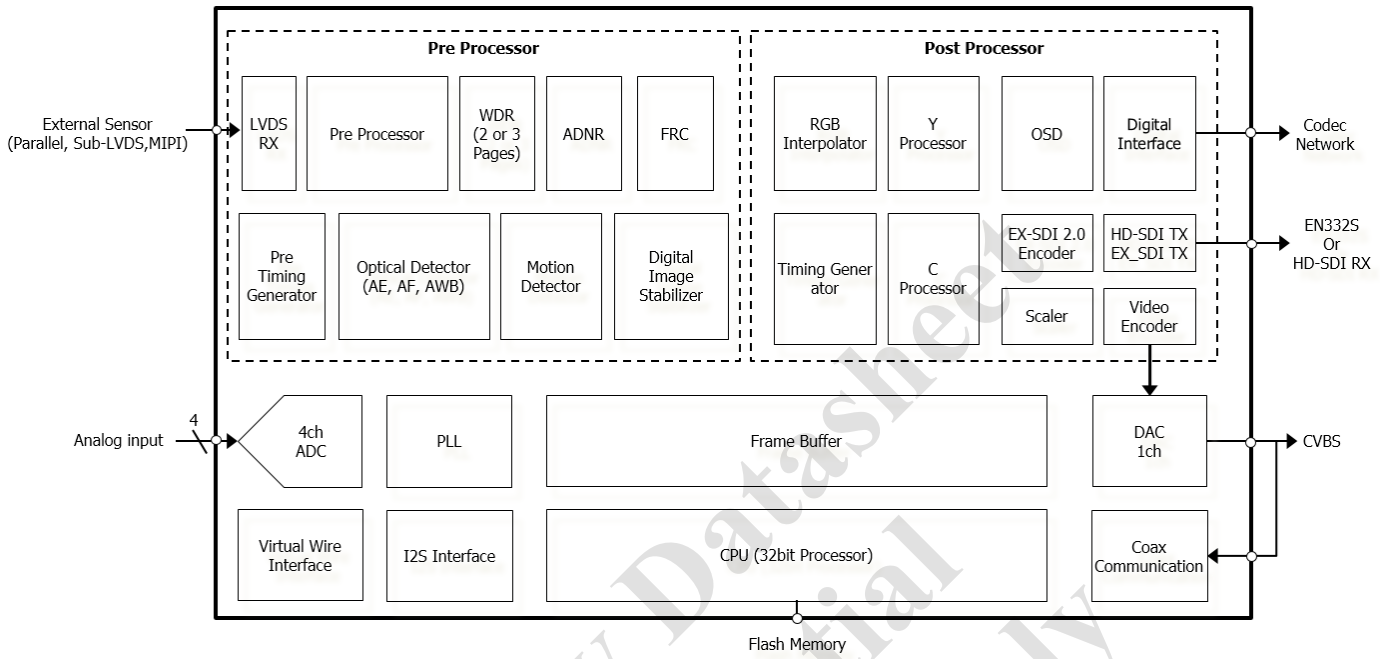
L8	SFDQ0	IO	External Serial flash data0		
M8	SFDQ1	IO	External Serial flash data1		
L9	SFDQ2	IO	External Serial flash data2		
M9	SFDQ3	IO	External Serial flash data3		
M10	SFCSN	O	External Serial flash chip select		
K7	GPIO0	IO	General purposed IO	External IRQ0	
L6	GPIO1	IO	General purposed IO	External IRQ1	
L7	GPIO2	IO	General purposed IO	PWM0 (CAP0)	
M7	GPIO3	IO	General purposed IO	PWM1 (CAP1)	
A6	GPIO4	IO	General purposed IO	RXD1	
A7	GPIO5	IO	General purposed IO	TXD1	
C1	GPIO6	IO	General purposed IO	SPI_CS1	
C5	GPIO7	IO	General purposed IO	SPI_DO1 (TWI_SDA2)	
C6	GPIO8	IO	General purposed IO	SPI_CK1 (TWI_SCL2)	
K2	GPIO9	IO	General purposed IO	SPI_CS2	
K1	GPIO10	IO	General purposed IO	SPI_DO2	
L1	GPIO11	IO	General purposed IO	SPI_CK2	
M1	GPIO12	IO	General purposed IO	SPI_DI2	
C7	GPIO13	IO	General purposed IO	SPI_DI1	
A3	GPIO14	IO	General purposed IO		ENC_CK
L2	GPIO15	IO	General purposed IO	TWI_SCL	
M2	GPIO16	IO	General purposed IO	TWI_SDA	
M6	GPIO17	IO	General purposed IO		EX-SDI UCC
K4	GPIO18	IO	General purposed IO	PWM2 (CAP2)	
K3	GPIO19	IO	General purposed IO	PWM3 (CAP3)	
M3	GPIO20	IO	General purposed IO	PWM4 (CAP4)	I2S output
L3	GPIO21	IO	General purposed IO	PWM5 (CAP5)	I2S input
B4	GPIO22	IO	General purposed IO		I2S WCK
A4	GPIO23	IO	General purposed IO		I2S BCK
J3	GPIO24	IO	General purposed IO		Virtual wire 0
L4	GPIO25	IO	General purposed IO		Virtual wire 1
M5	GPIO26	IO	General purposed IO		Virtual wire 2
M4	GPIO27	IO	General purposed IO		Virtual wire 3
L5	GPIO28	IO	General purposed IO		
K6	GPIO29	IO	General purposed IO		
K5	GPIO30	IO	General purposed IO		FLD out

C8	GPIO31	IO	General purposed IO		Logic PWM out
B5,B6,B7, B8,G7,H6	VDDC	IO	Core power 1.2V (Digital)		
D6	AVDD_LVPLL	IO	Sub-LVDS / PLL power 1.2V (Analog)		
C11	AVDD_SDI	IO	HD-SDI power 1.2V (Analog)		
C2	VDDQ_SS	IO	Sensor I/F IO power 1.8V ~ 3.3V (Digital)		
A5,H7	VDDQ_DDR	IO	DDR memory IO / Core power 1.8V (Digital)		
D8,E8,E9	VDDQ_BT	IO	BT1120 IO power 1.8V ~ 3.3V (Digital)		
F8,G8,H8	VDDQ	IO	IO power 3.3V (Digital)		
D5	AVDD_LV33	IO	Sub-LVDS power 3.3V (Analog)		
D9	AVDD_SDI33	IO	HD-SDI power 3.3V (Analog)		
B12, D1, D2, D3, D4, E5, E6, E7, F5, F6, F7, G5, G6, H5, J4	GND	IO	Ground		

3.2 I/O Power Information

Power Name	I/O	Related IO	Voltage
VDDQ_SS	P	MCKO,HSI,VSI,PCLK,GPIO6/7/8/13	1.8V
AVDD_LV33	P	LDIP0~7, LDIM0~7,LDIPCK,LDIMCK	3.3V
VDDQ_BT	P	YO0~9,CO0~9,HSO,VSO,DCKO,DENO	1.8V~3.3V
AVDD_SDI33	P	SDIM,SDIP	3.3V
VDDQ	P	ADCI0~3,CVBS,JMODE,JTRST,JTDO,JTMS,JTDI,JTCK TP0~2,RSTX,XI0~1,EXTS,SFCSN,SFCKO,SFDQ0~3,RX0,TX0,GPIO0~5,GPIO9~12, GPIO14~31	3.3V

4. Block Diagram



CMOS Image sensor has RGB Bayer structure, so the input image must be RGB Bayer structured format (resolution 1.3-4Mpixel). The output from the DSP has three forms: Embedded HD-SDI as Main output, Digital YC (4:2:2) output, and CVBS Analog output is the other.

DSP consists of Pre-Processor, Post-Processor and CPU.

1. Pre Processor performs Digital Clamping, Defect Correction, and Shading Compensation and then performs WDR and then 2D/3D DNR. The DNR output image is then sent to Post-Processor.
   In addition, AE, AF, AWB Optical Detector for feature and motion detection function are also performed.

2. Post Processor uses DDR SDRAM to transmit images to next stage. SDRAM is used to provide synchronization between Pre Processor and Post Processor. The Digital Zoom function is also performed together.

3. Post Processor consists of RGB Interpolator, Y / C Processor, OSD (Privacy, Font, and Test). In addition, it also consists of Timing Generator which controls the output timing.

This module also includes HD-SDI TX, Video Encoder, DAC, Sub-LVDS, ADC and PLL, etc.

5. Function Description

5.1 RGB Interpolator

This function converts 3 channel RGB to RGB Bayer Pattern. The most important goal of this function is to correct unknown pixel. For this, it is including the following features internally.

- Diagonal frequency compensation Filter
- Minimize mosaic pattern

5.2 Wide Dynamic Range compensation (WDR)

This is the ability to expand the dynamic range. This function uses alternative exposure time control method.

- Dual shutter image fusion (Max. 90dB)
- Line by Line WDR (Max. 120dB)
- Based on Bayer pattern
- Spatial adaptive gamma correction

5.3 Digital Noise Reducer (2D/3D)

This feature removes noise in images (temporal domain). Temporal noise is reduced by 3D filter using frame memory. Especially,

- 2D noise reducer
- 3D noise reducer
- Based on Bayer pattern

5.4 Adaptive Contrast Enhancer (ACE)

This function is a local adaptive contrast enhancement. It uses a histogram analysis and tone mapping method in pixel domain.

- Individual histogram equalization
- Temporal IIR filter
- Adjustable with input image level

5.5 Lens Shading Compensation

This function compensates shading effect caused by lens. It uses 2D shading table for compensation.

5.6 Defect Detection & Correction

This function corrects the defect of image at run-time. It supports only auto modes.

- Auto detection method
- Edge adaptive defect correction

5.7 Optical detector (AE, AF, AWB)

This function detects optical characteristics.

- AE Detector
  Detection Window: 6ea
  Integration of Luminance result and pixel counter in each window
  Histogram of input image (variable detection level)
  Limitation of integration through Clip/Slice control
- AF Detector
  Detection Window: 2ea
  Integration of the Band Pass Filter output of image and counter in each window
  Line Peak and pixel counter
  Cut Off Frequency: 6step
  Noise Slice
  BPF: FIR filter
  Vertical filter
  Spot Image detection filter
- AWB Detector
  Detection Window: 1ea
  White Zone Detector: Color Map method
  Integration of each R, G, B and pixel counter
  Counter of saturated Pixels

5.8 Edge enhancement

This function enhances the edges of image for sharpness.

- Adjustment edge gain/threshold/limit
- Control negative/positive edge
- Noise slicing and detection of high frequency edge

5.9 Gamma Correction

- Gamma control point : 16 point
- 2 gamma tables are controlled at the same time.
- Fixed point on X-axis
- Control each Y/C

5.10 Hue Controller

This function adjusts the hue of image.

- Direction gain control with 8 directions
- Hue control with 8 directions

5.11 Pseudo Color Suppression

This function has the ability to suppress the color.

- High light color suppression
- Low light color suppression
- Edge color suppression

5.12 High Light Masking

This is the ability to mask the high light zone with specific color & level.

5.13 Box OSD (32ea, solid effects)

- OSD quantity : 32ea
- Blending effect : 4step
- Box border : solid effects
- Auto zoom position function

5.14 Font OSD

This function displays MENU for camera.

- Font size: 16 x 24 pixel (Max. 341 characters)
- Scaling of each H,V
- Line return, page return
- Blending effects with 4 steps
- 4 font color palettes
- Adjustment of character space
- Supports half character size

5.15 Motion Object Detector

This function detects the moving objects in image

- Detecting resolution: 32x32 pixels
- Detecting object size: Variable

5.16 External Audio Interface

EN779 supports external audio interface, I2S in / output

- I2S Decoder/Encoder

6. CPU Specification

6.1 CPU General Description

The CPU in this device is operated with an external flash memory. It supports the quad type serial flash memory.

6.2 CPU Features

High-performance, low-power 32-bit ExRISC 1.0 processor

32-bits ExRISC 1.0 Architecture

- Instructions compatible with ExRISC 1.0 processor
- Max. 74.25 MHz
- 7 stage pipelines including branch prediction and pre-fetch units
- 32 GPRs
- 16 KB instruction cache, 8 KB data cache

Embedded Memory

- 32 KB internal SRAM x 4

Special Function

- Serial flash memory access
  - Support quad, single data access

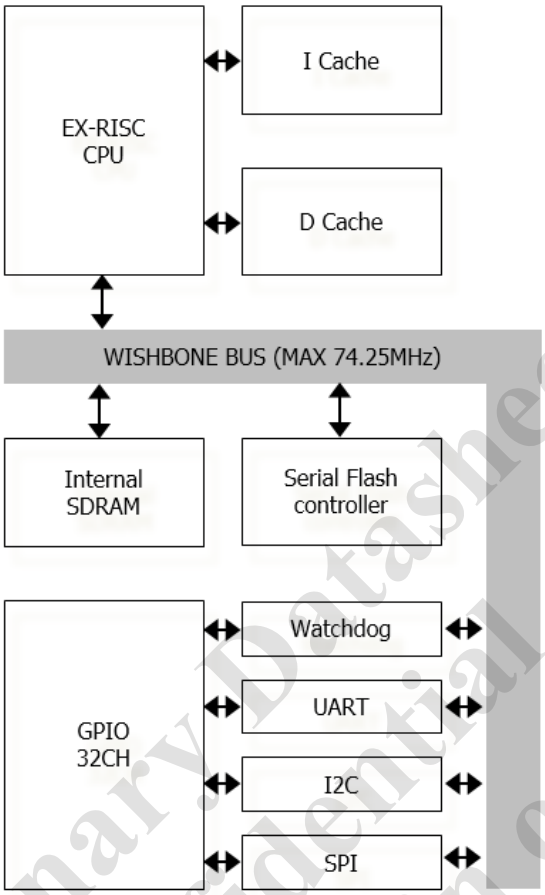
Peripherals

- 2ch UART
- 32ch GPIO with second function
- 2ch I2C controller
- 2ch SPI
- 6ch timer with PWM output
- 32bit counter Watchdog function

Operating frequency

- Max. 74.25 MHz

6.3 CPU Block Diagram



6.4 Address map

Address	Function
0xF0000000	Serial flash controller
0xF1000000	UART controller
0xF2000000	GPIO controller
0xF3000000	I2C controller
0xF4000000	SPI0 controller
0xF5000000	SPI1 controller
0xF6000000	TIMER / PWM controller
0xF7000000	Watchdog timer controller

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

(I/O Power: 1.8V / 3.3V)

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
VDDC	DC Internal Voltage	1.08	1.2	1.32	V
VIN	DC Input Voltage(1.8V)	1.65	1.8	1.95	V
	DC Input Voltage(3.3V)	3.0	3.3	3.6	V
VOUT	DC Output Voltage(1.8V)	1.65	1.8	1.95	V
	DC Output Voltage(3.3V)	3.0	3.3	3.6	V

7.2 Recommended Operating Conditions

Symbol	Parameter	Rating	Unit
VDDC	DC Internal Voltage	1.2V±0.12	V
VIN	DC Input Voltage(1.8V)	1.8V±0.18	V
	DC Input Voltage(3.3V)	3.3V±0.33	V
VOUT	DC Output Voltage(1.8V)	1.8V±0.18	V
	DC Output Voltage(3.3V)	3.3V±0.33	V
TOPR	Operating Temperature	0 to 70 (TBD)	℃
TSTG	Storage Temperature	-40 ~ 125 (TBD)	℃

7.3 Static Characteristics

	Level			Unit	Note
	Pin	Target	Ref.		
Human Body Model	All	±2,000 ↑		V	TBD
Charged Device Model	All	±500 ↑		V	TBD

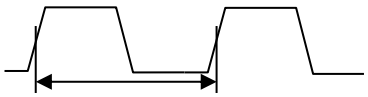
7.4 DC Electrical Characteristics

Item		Pins	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Analog	AVDD_SDI	$AVDD_{SDI}$		1.08	1.2	1.32	V
		AVDD_SDI33	$AVDD_{SDI33}$		3.0	3.3	3.6	V
		AVDD_LVPLL	$AVDD_{LVPLL}$		1.08	1.2	1.32	V
		AVDD_LV33	$AVDD_{LV33}$		3.0	3.3	3.6	V
	Digital	VDDQ	VDDQ		3.0	3.3	3.6	V
		VDDQ_BT	$VDDQ_{BT}$		1.7/3.0	1.8/3.3	1.95/3.6	V
		VDDQ_SS	$VDDQ_{SS}$		1.7	1.8	1.95	V
		VDDQ_DDR	$VDDQ_{DDR}$		1.7	1.8	1.95	V
		VDDC	VDDC		1.2	1.26	1.32	V
Digital input voltage		LDIM0~7 LDIP0~7 LDIMCK LDIPCK	$\triangle V_{LCM}$		-25		25	mV
			$\triangle V_{LD}$		-25		25	mV
			V_{LD}		100	150	200	mV
			Z_{dif}		98	100	102	Ω
			V_{LCM}		0.8	0.9	1	V
		RSTX, XI0, XI1, TP0~2, GPIO0~5, GPIO9~12, GPIO14~31, RX0, SFDQ0~3, JMODE, JTRST, JTMS, JTDI, JTCK	VIH		0.7 VDDQ		4	V
			VIL		-0.3		0.3 VDDQ	V
		VSO, HSO	VIH_{BT}		0.7 $VDDQ_{BT}$		4	V
			VIL_{BT}		-0.3		0.3 $VDDQ_{BT}$	V
		PCLK, VSI, HSI, GPIO6, GPIO7, GPIO8, GPIO13	VIH_{SS}		0.7 $VDDQ_{SS}$		4	V
			VIL_{SS}		-0.3		0.3 $VDDQ_{SS}$	V
Digital output voltage		GPIO0~5, GPIO9~12, GPIO14~31, TX0, SFDQ0~3, SFCKO, SFCSN, JTDO	VOH		VDDQ-0.2			V
			VOL				0.2	V
		DCKO, DENO, VSO, HSO, YO0~9, CO0~9	VOH_{BT}		$VDDQ_{BT}$-0.2			V
			VOL_{BT}				0.2	V
		MCKO, VSI, HSI, GPIO6, GPIO7, GPIO8, GPIO13	VOH_{SS}		$VDDQ_{SS}$-0.2			V
			VOL_{SS}				0.2	V
Serial output Voltage (Common)		SDIP, SDIM	V_{CMO}	REXTH=750Ω HD mode		$AVDD_{SDI33}$ - $\triangle V_{SDO}/2$		V

7.5 AC Electrical Characteristics

1) Main reference clock

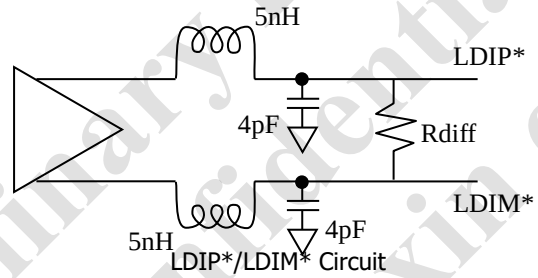
CLK



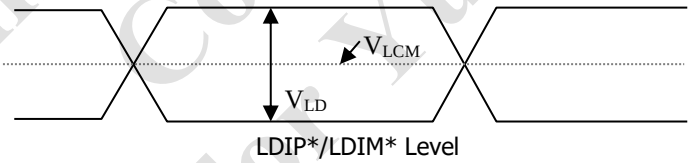
37.037ns (Frequency 27MHz)

2) Input LVDS data characteristics

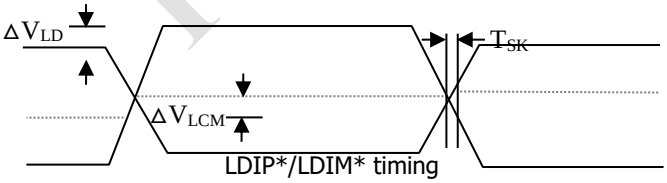
Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential motion skew time	T_{SK}			100	ps
Duty ratio	T_H/T_L	45	50	55	%
DDR clock frequency	f				MHz



LDIP*/LDIM* Circuit



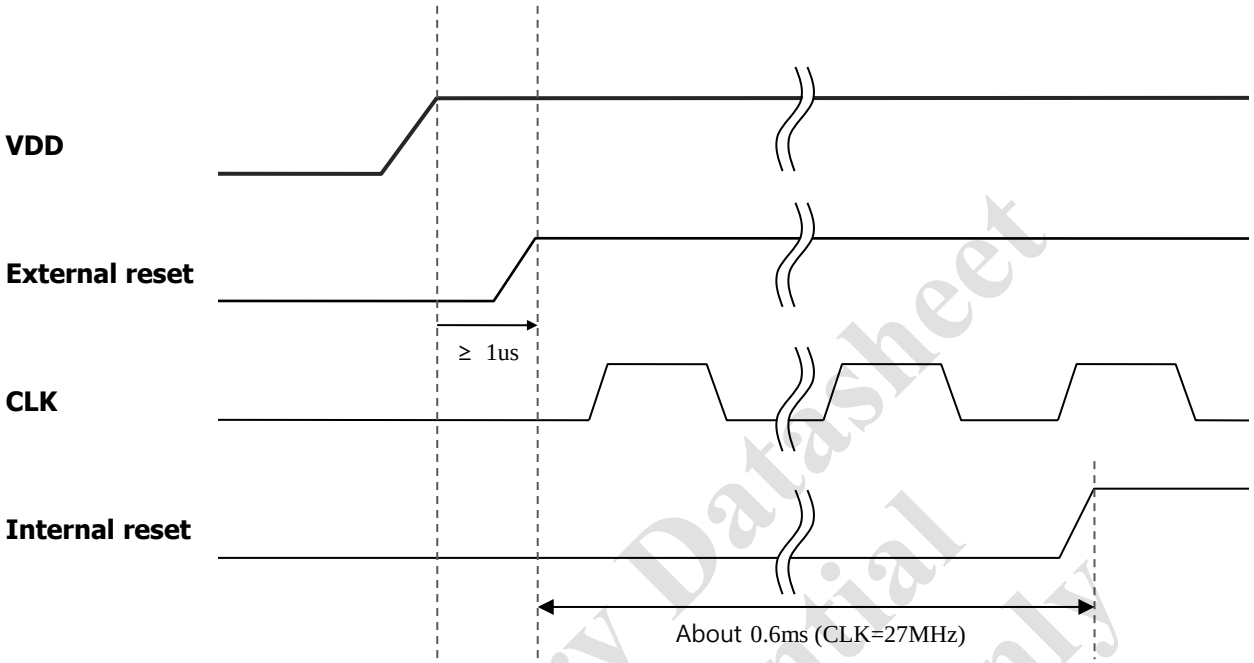
LDIP*/LDIM* Level



LDIP*/LDIM* timing

8. Power on Sequence

8.1 Power, Reset and Clock



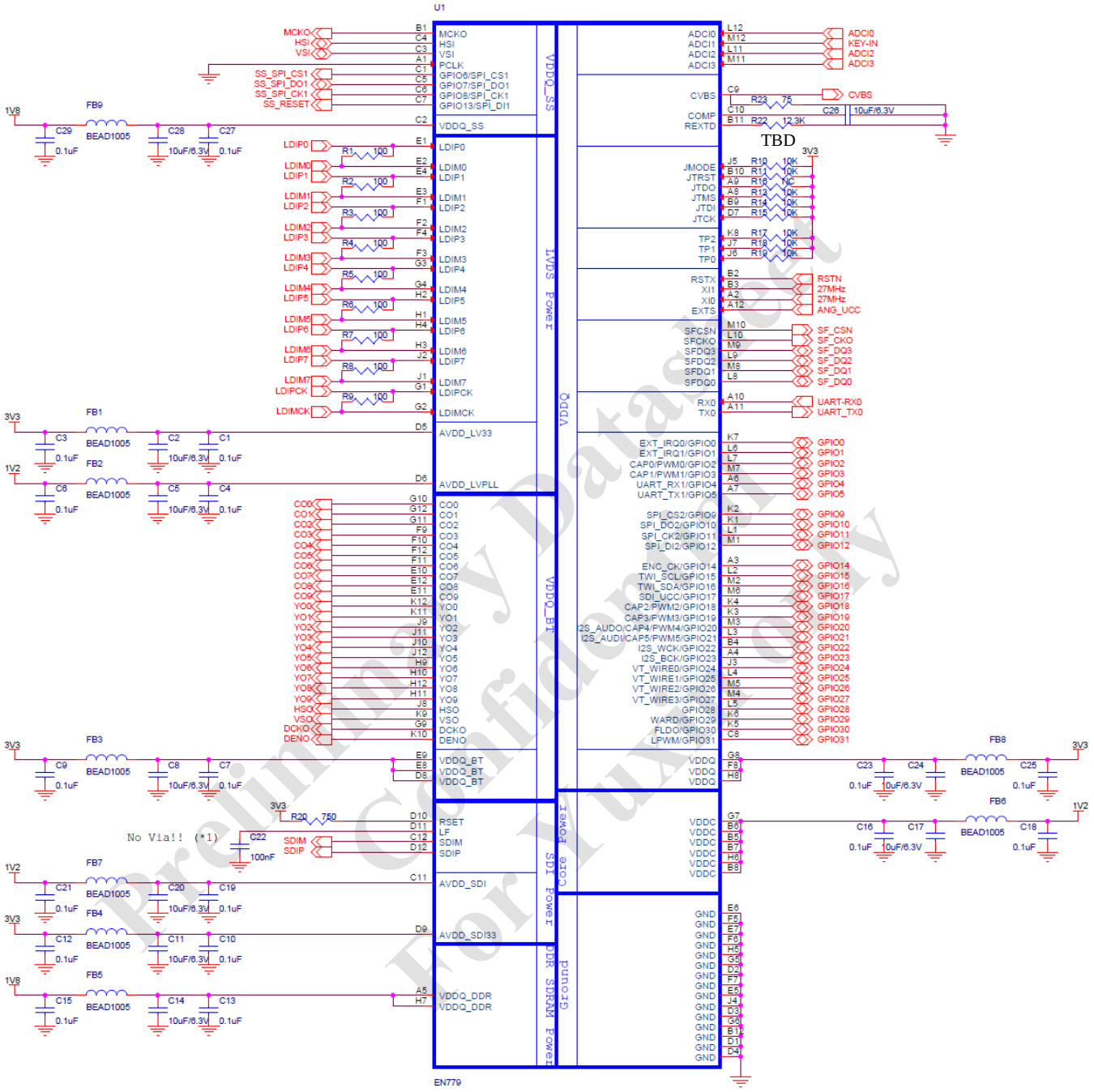
After power on, and when external reset is "High", CLK comes in and internal reset will be "high" after 1200 us (CLK at 27 MHz standard). All processes will work when the internal reset is high.

9. Power Consumption

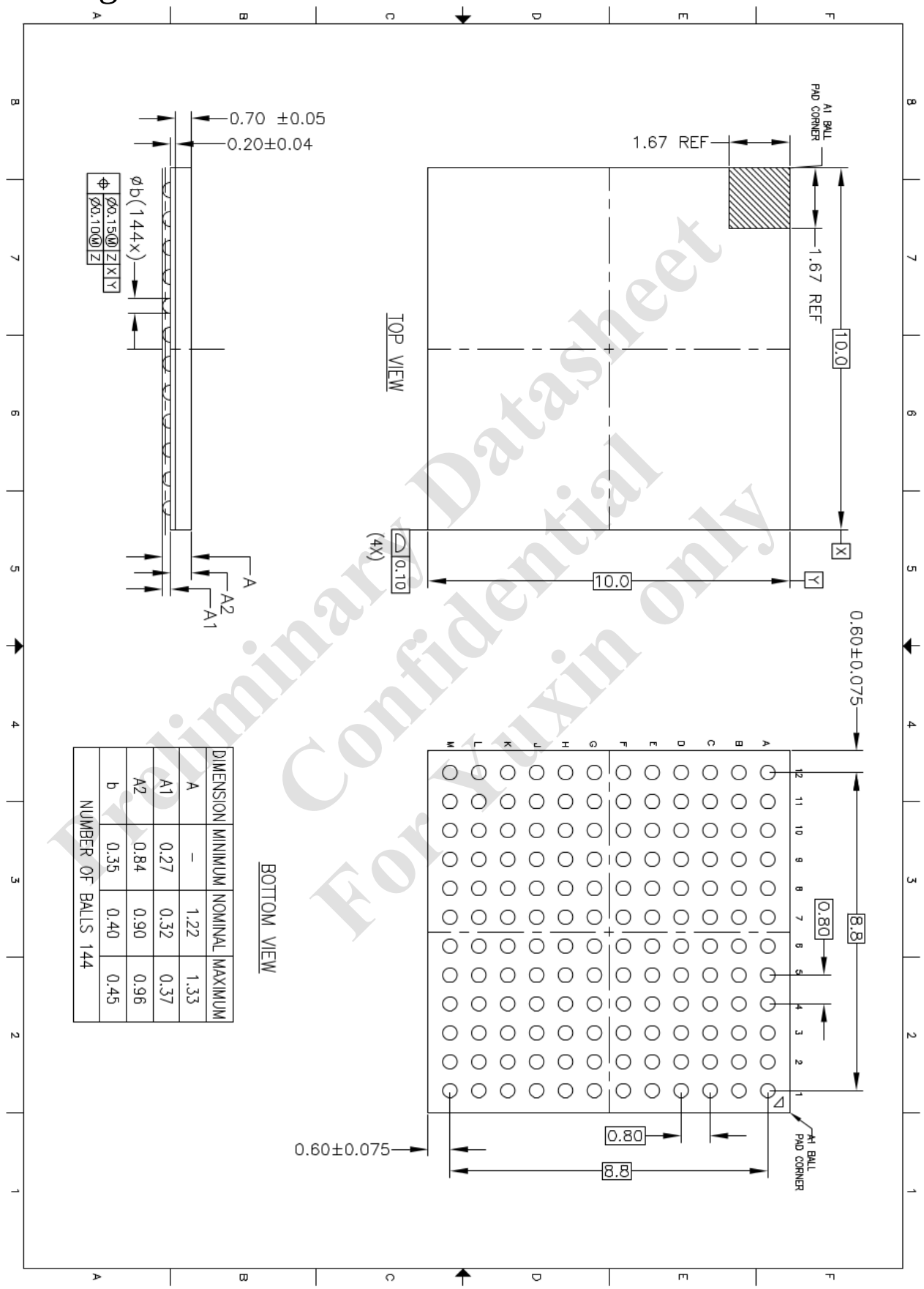
	VDDQ	AVDD_SDI33	AVDD_LV33	VDDQ_DDR	VDDQ_SS	VDDC	AVDD_LVPLL	AVDD_SDI	VDDQ_BT	Total (mW)
	3.3V	3.3V	3.3V	1.8V	1.8V	1.2V	1.2V	1.2V	3.3V	
4MP 30P	71.28	1.32	11.55	113.04	1.8	675.6	3	18.36	164.67	1060.62

Note)
It is not all function operation.
It is measurement value.

10. Basic Schematic



12. Package Dimension



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	–	1.22	1.33
A1	0.27	0.32	0.37
A2	0.84	0.90	0.96
b	0.35	0.40	0.45
NUMBER OF BALLS 144			